Distributed Sniffer Nodes for Batteryless Sensor Nodes (sdmay24-25)

Website

https://sdmay24-25.sd.ece.iastate.edu/

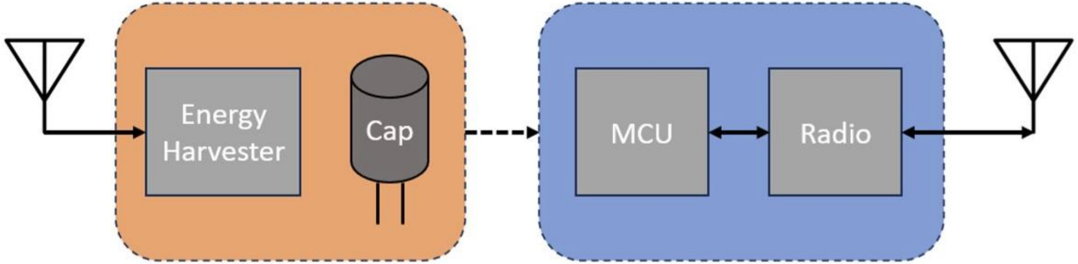
Team Lead/ Software Lead: Thomas Gaul
Hardware Lead: Tori Kittleson
Hardware Member: Matthew Crabb
Software Member: Spencer Sutton
Scribe/Software Member: Ian Hollingworth

Advisor/Client: Henry Duwe
CPRE/EE 491 Fall 2023

IOWA STATE UNIVERSITY

Project Overview

BOB Node - Batteryless sensor designed by client.



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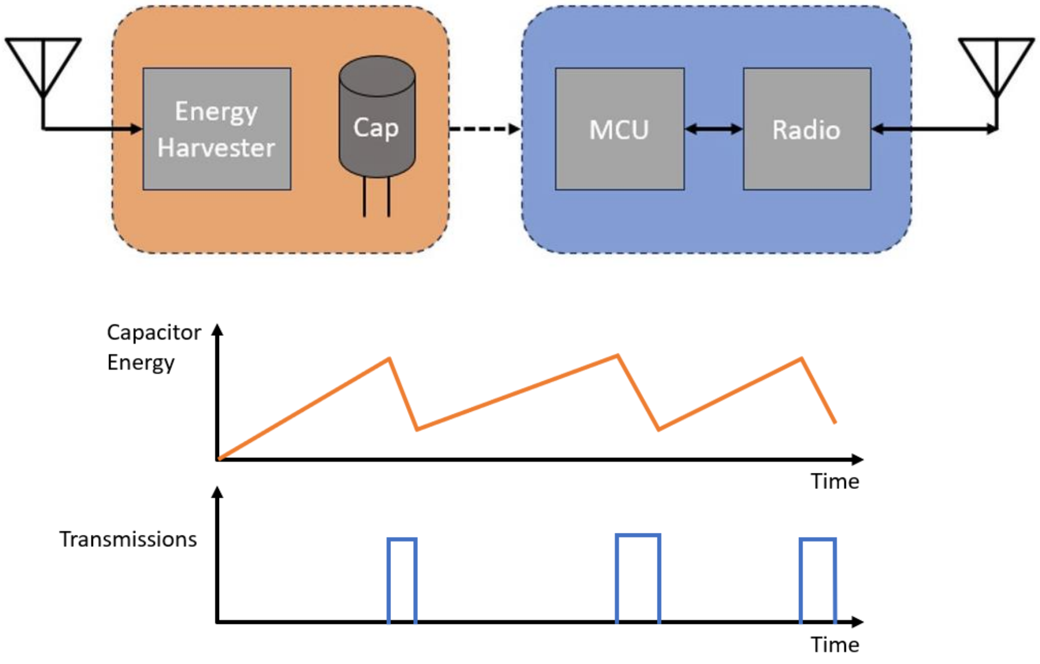
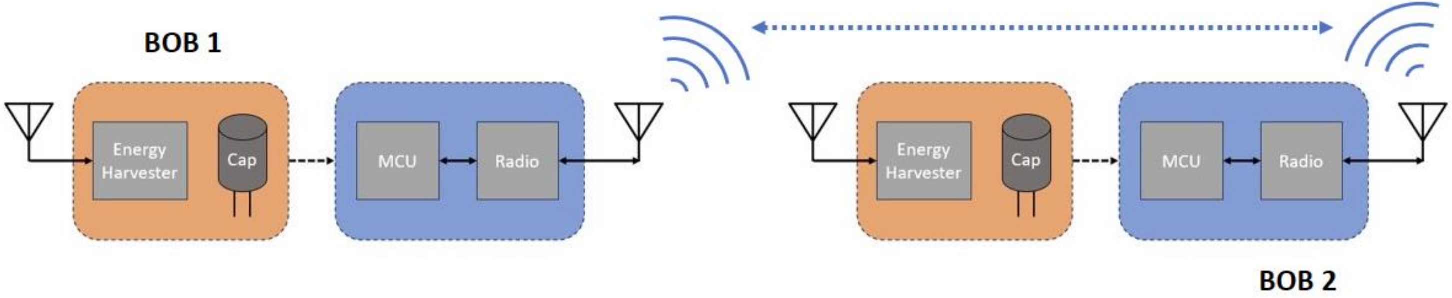
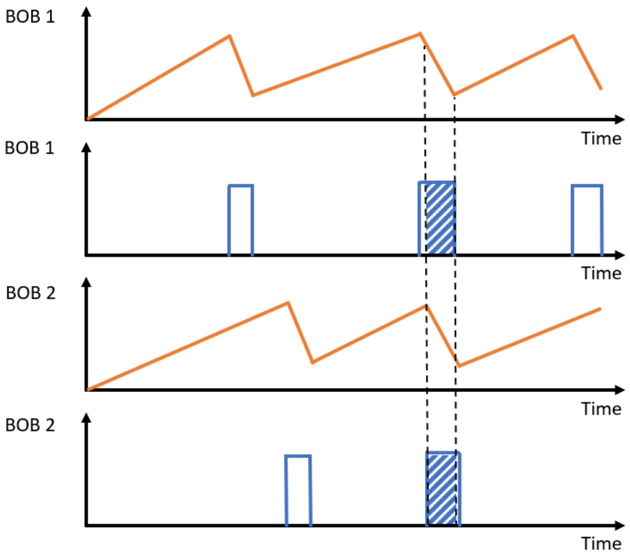
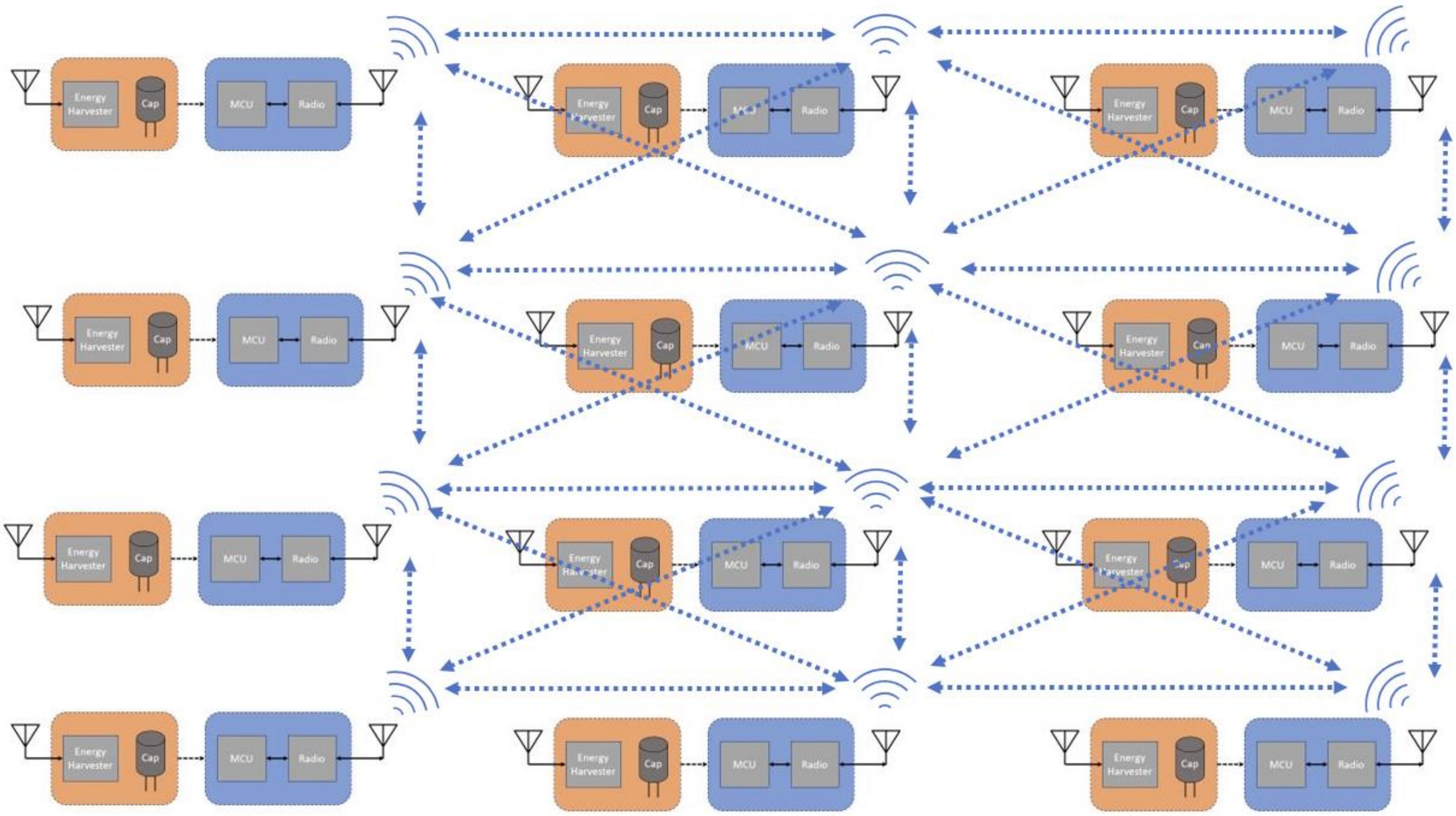
Project Overview



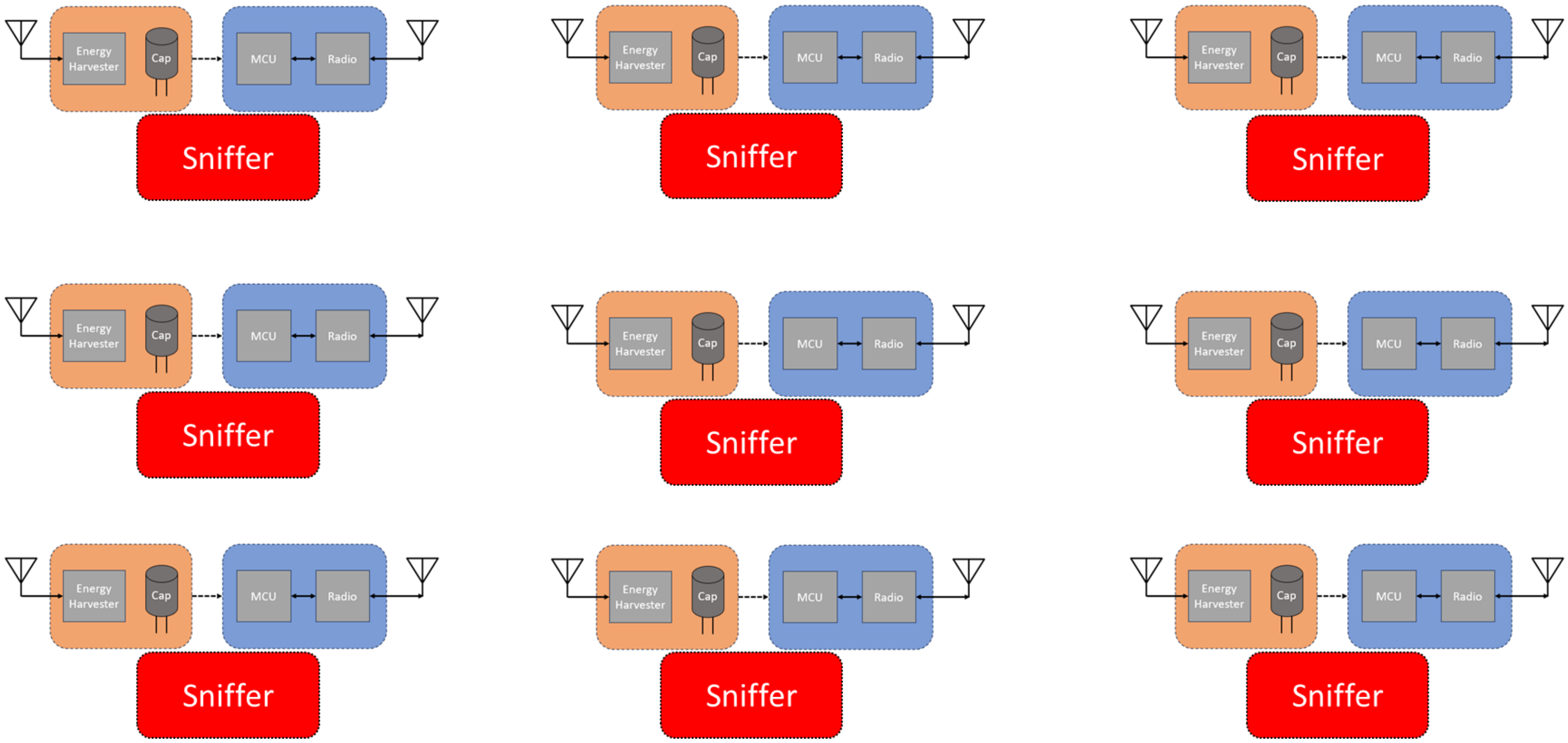

BOB 1
Energy Harvester
Cap
MCU
Radio
Energy Harvester
Cap
MCU
Radio
BOB 2


BOB 1
Time
BOB 1
Time
BOB 2
Time
BOB 2
Time



Energy Harvester
Cap
MCU
Radio

Goal: Create testbed for researchers to use for the batteryless nodes they are developing.



Use Cases

Scenario Node Tests

- Single node tests
- Multi-node and single lab testing (goal of 9)
- Large scale testing (goal of 100 – 1000)

Users

- Dr. Duwe's research group
- Universities, companies, hobbyists through open-source nature

Potential Impact

- Forest fire detection in national parks
- Factory condition monitoring
- Weather monitoring and recording

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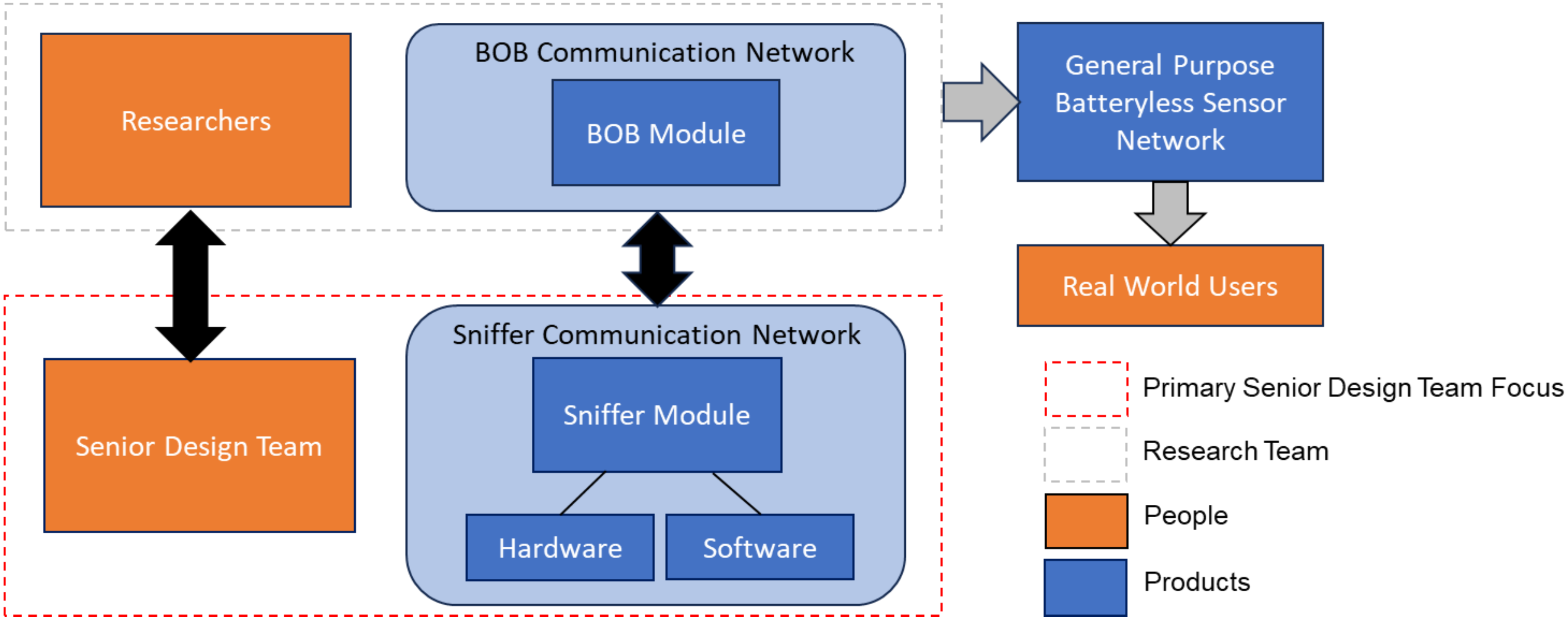
Visual Sketch



Requirements

Functional

- 9 BOB/Sniffer pairs
- Sink Sniffer Node with continuous power
- Host system to organize and store Sniffer logs
- Sniffer Nodes powered for one week
- Sniffer Nodes inflict minimal effects on BOB Nodes
- BOB Nodes electrically isolated from one another
- Modular stack of BOB and Sniffer custom boards

Non-functional

- Scalable for a potential larger (100+ node) design
- Documentation
- Mechanical durability of system

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Requirements

Engineering Standards

- UART communication protocol to connect Sink Sniffer Node to Host (RS-232)
- Radio communication standards (TI Proprietary 2.4 GHz)
- Bluetooth™ (IEEE 802.15.1)
- PCB design Standards

Deliverables

- Breakout Board Hardware
- MSP Simplified Hardware
- Sniffer Node Hardware
- Sniffer Node Software
- Open-Source Documentation
- Mechanically Sound System

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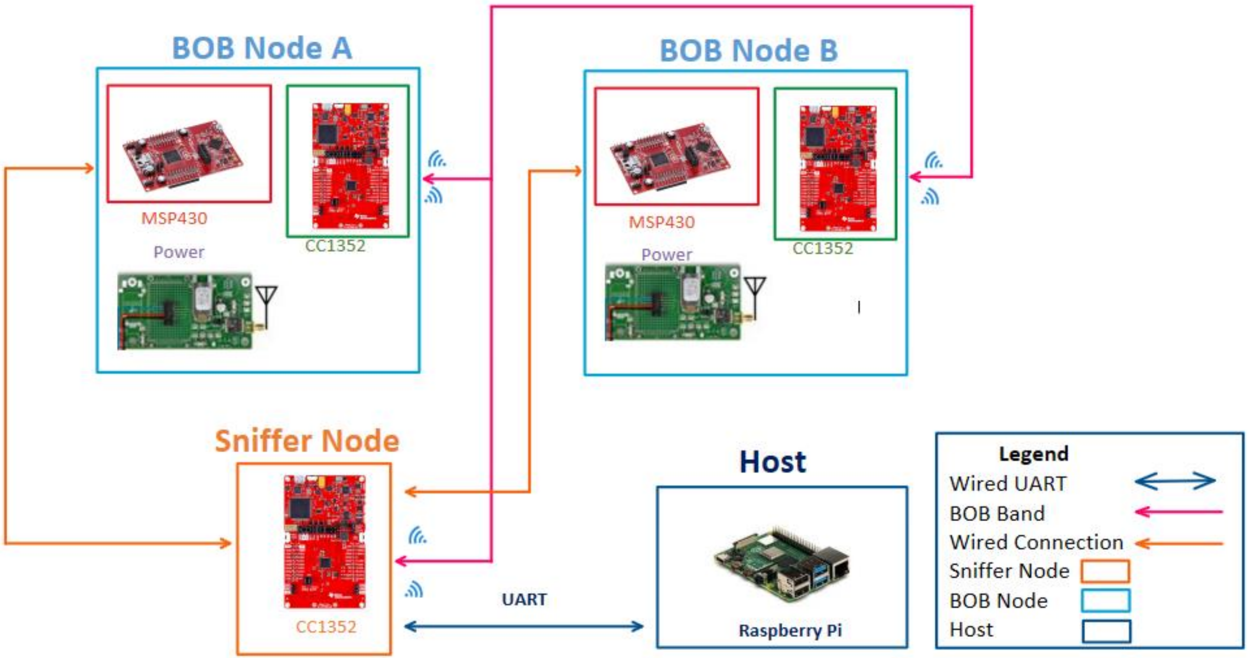
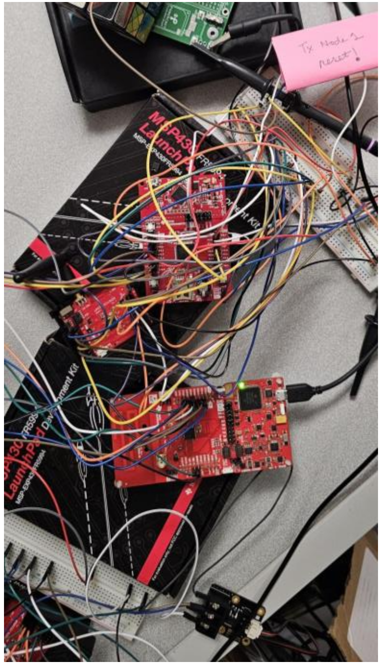
Current Design





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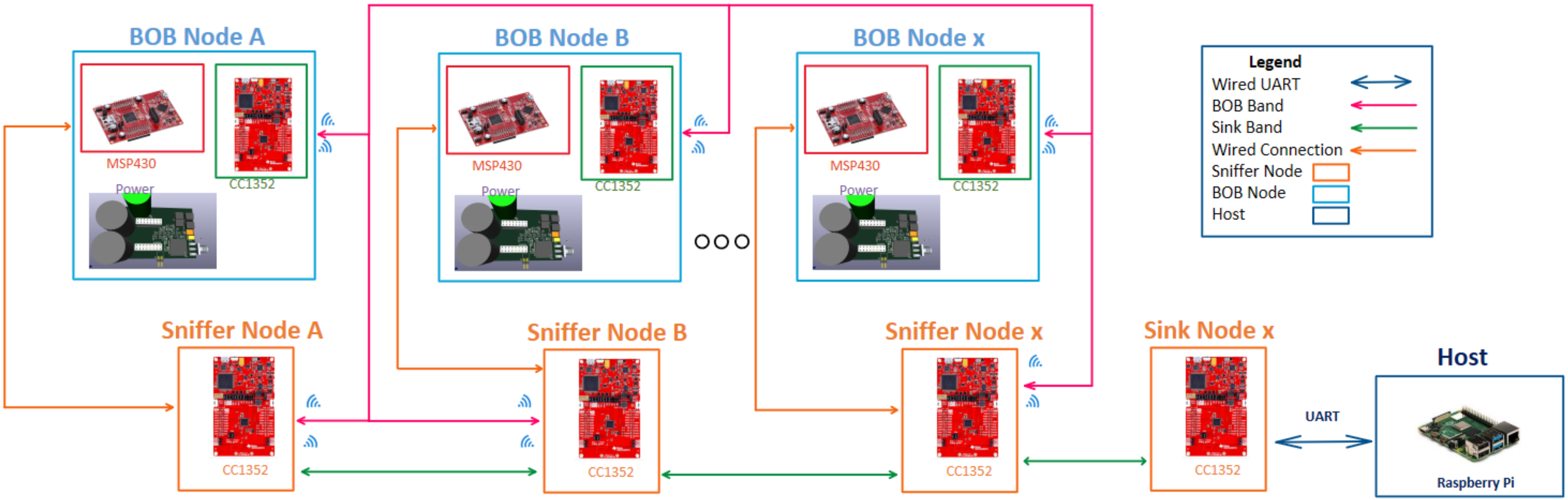
System Design



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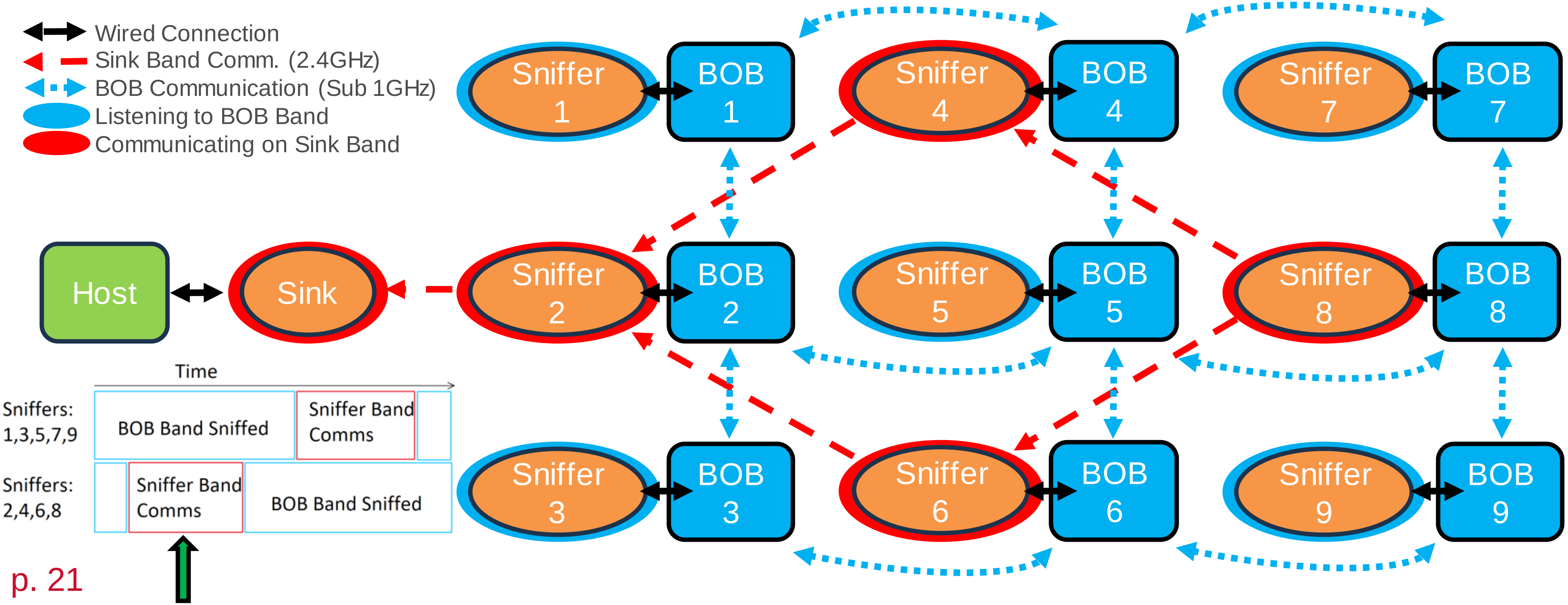
System Design



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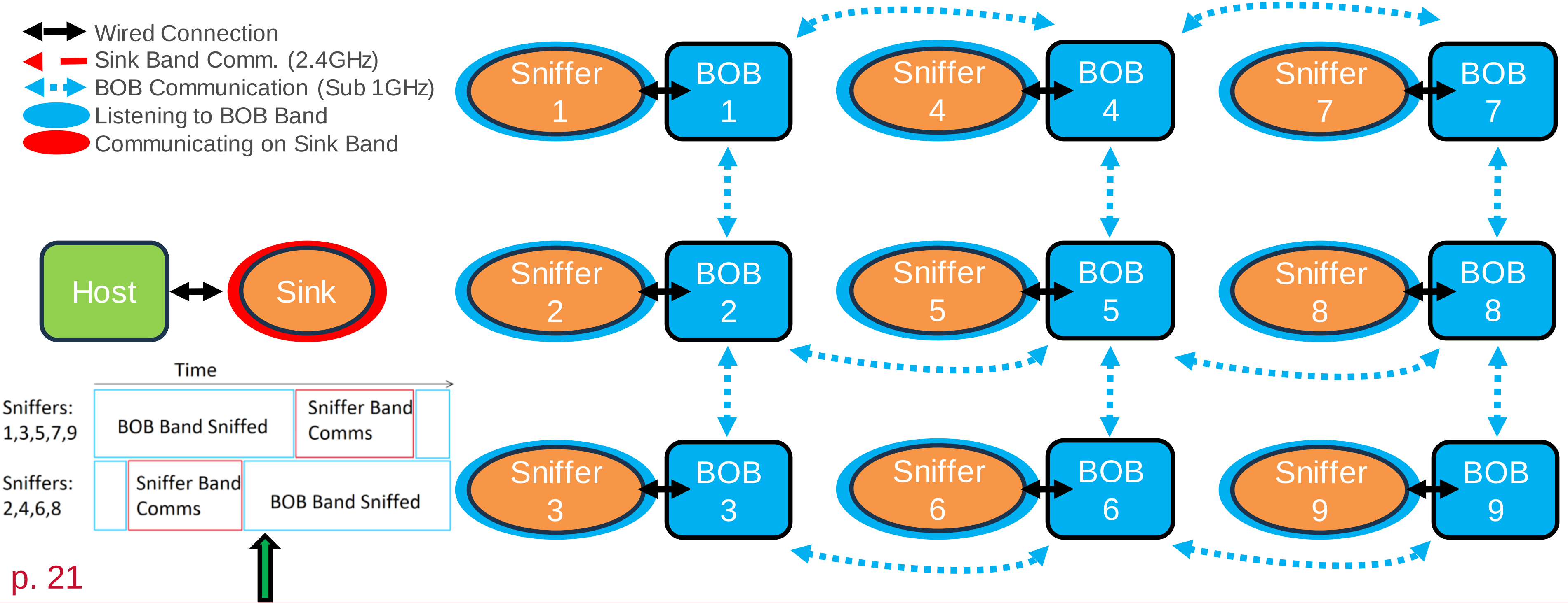
System Design



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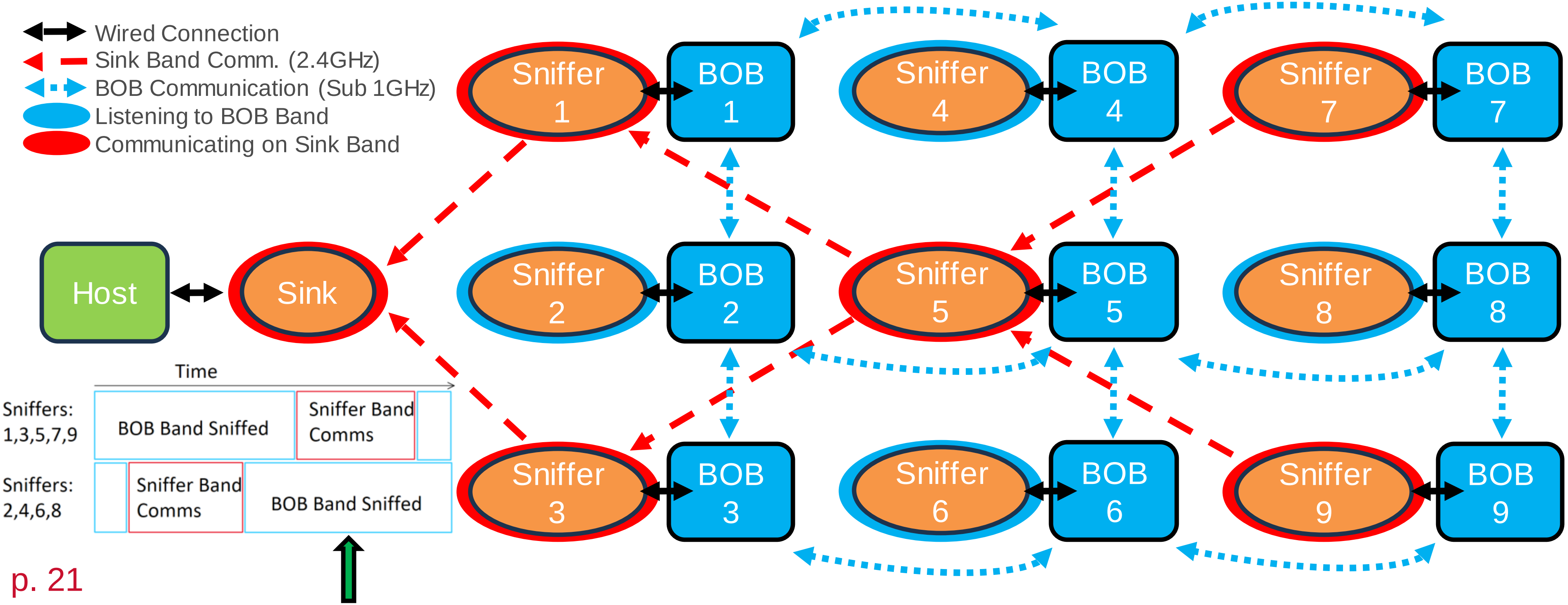
System Design



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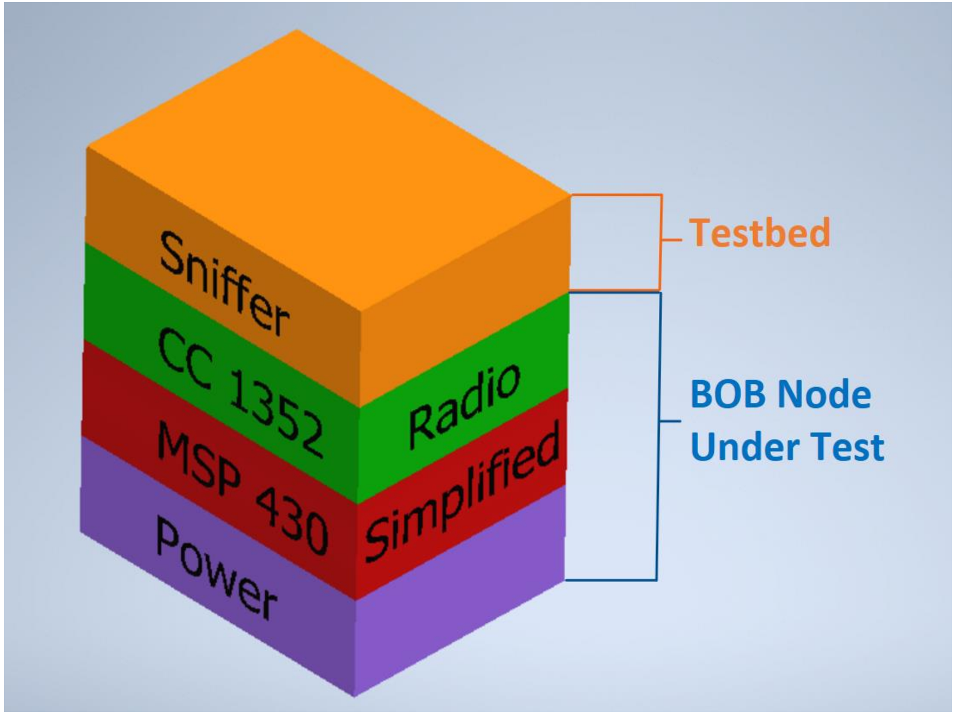
System Physical Design



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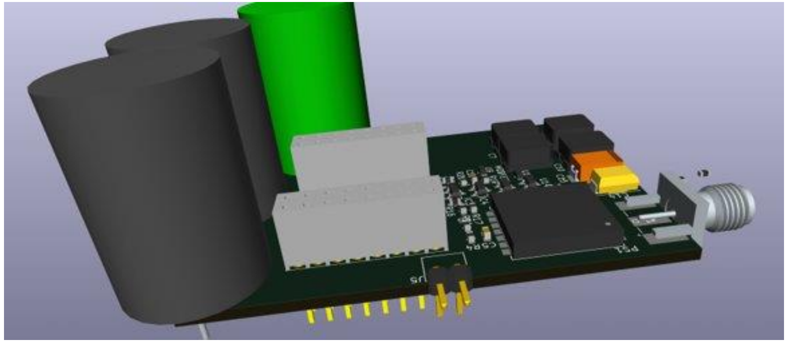
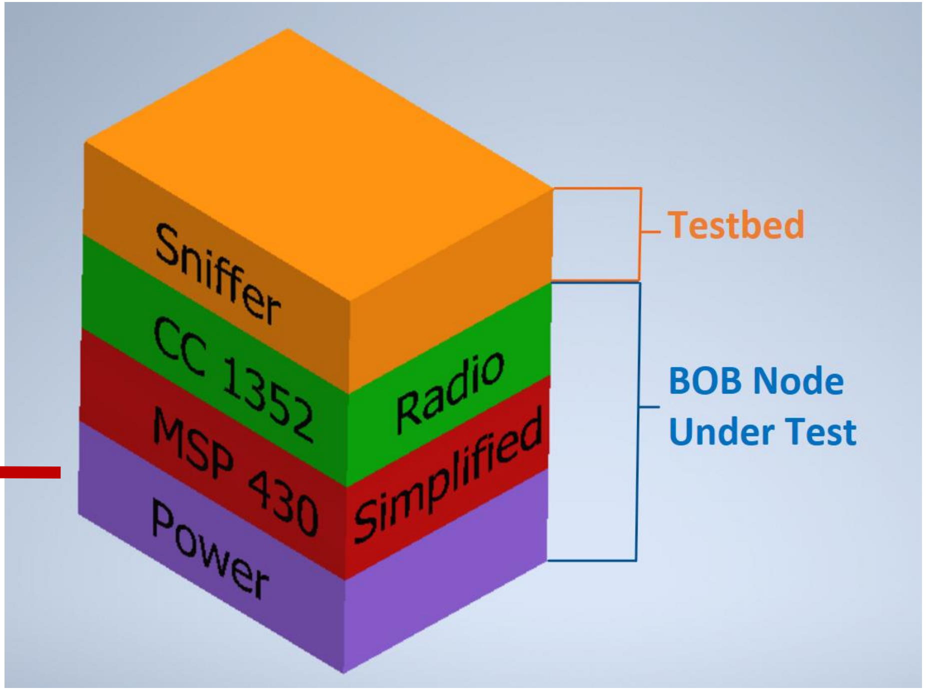
System Physical Design





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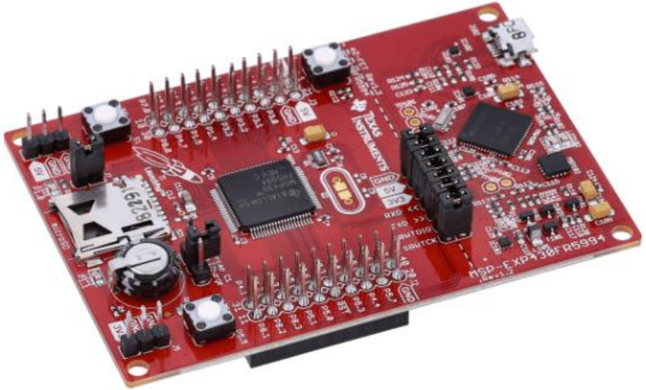
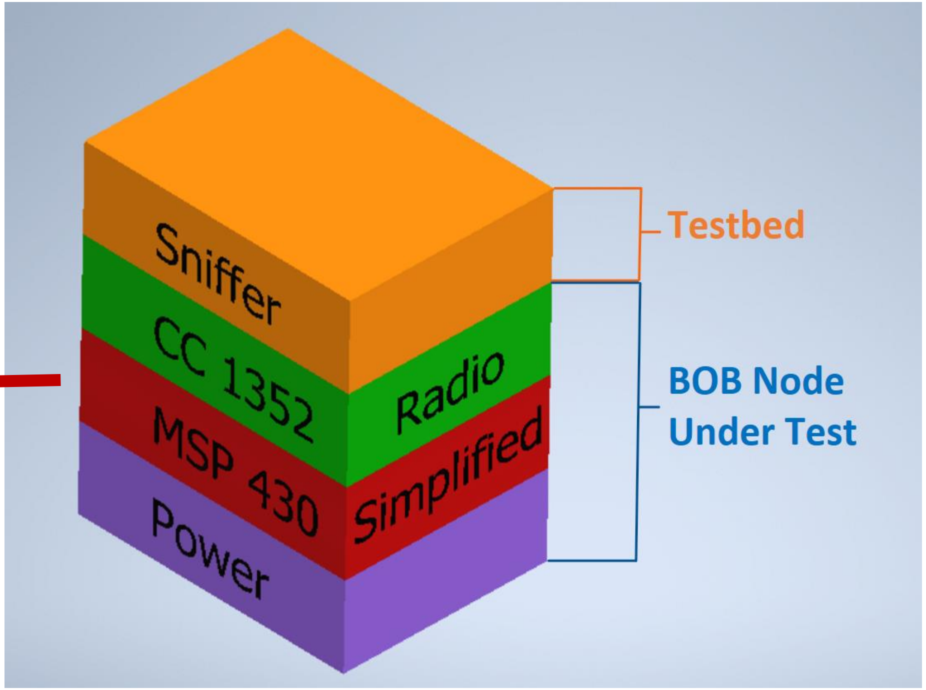
System Physical Design





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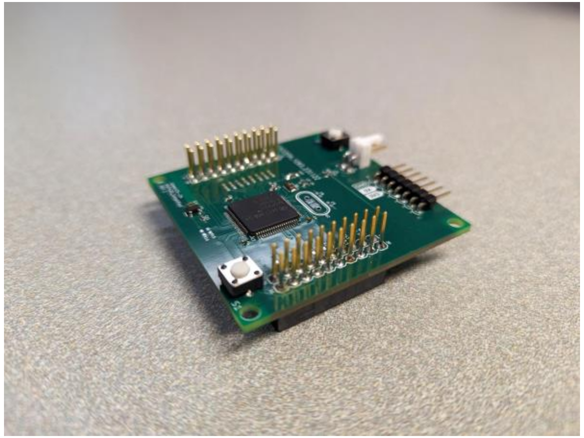
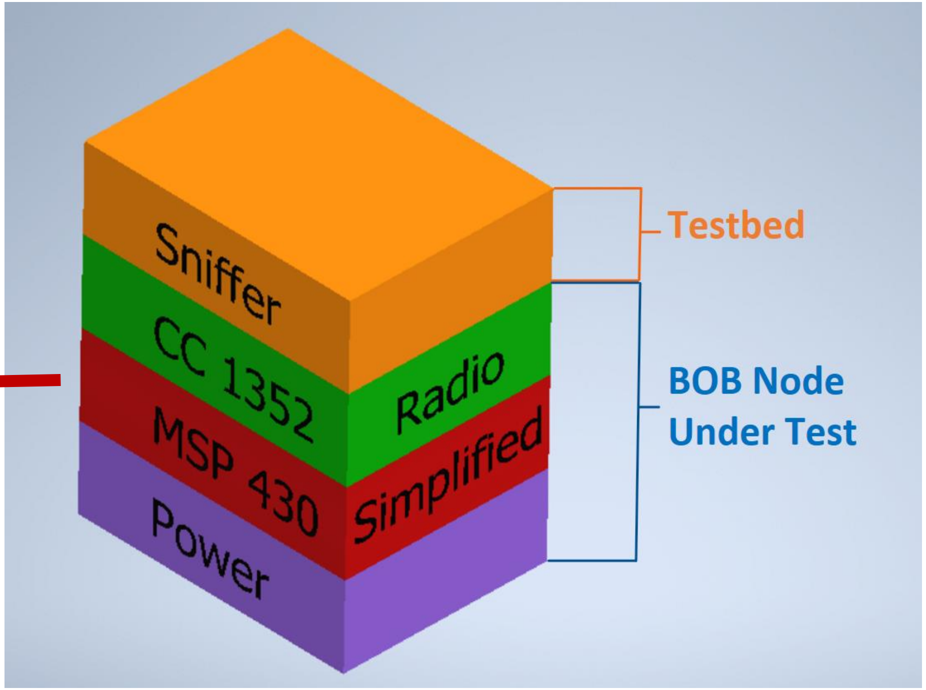
System Physical Design





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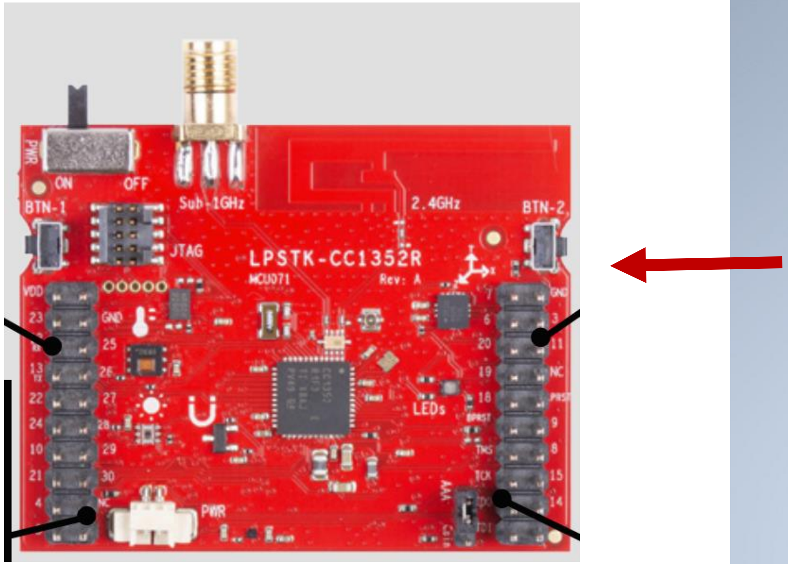
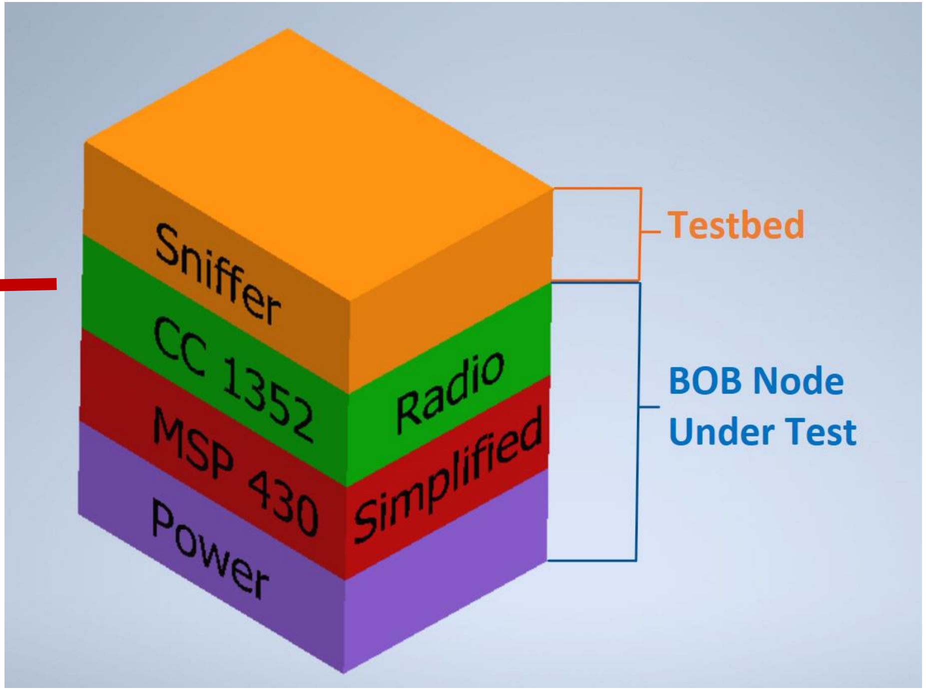
System Physical Design





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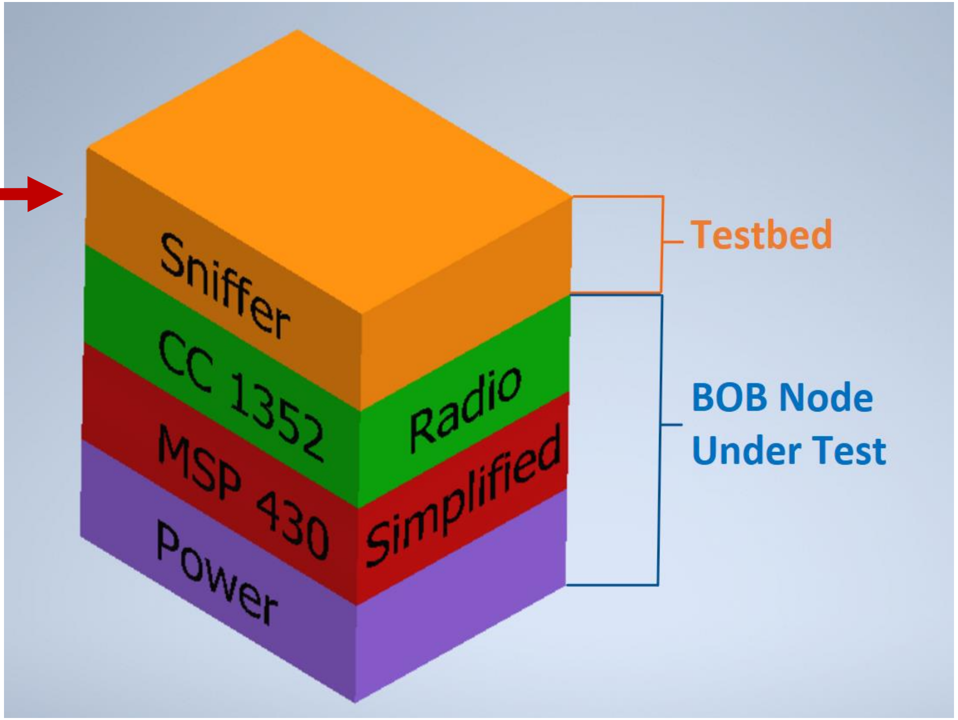
System Physical Design

Our Design



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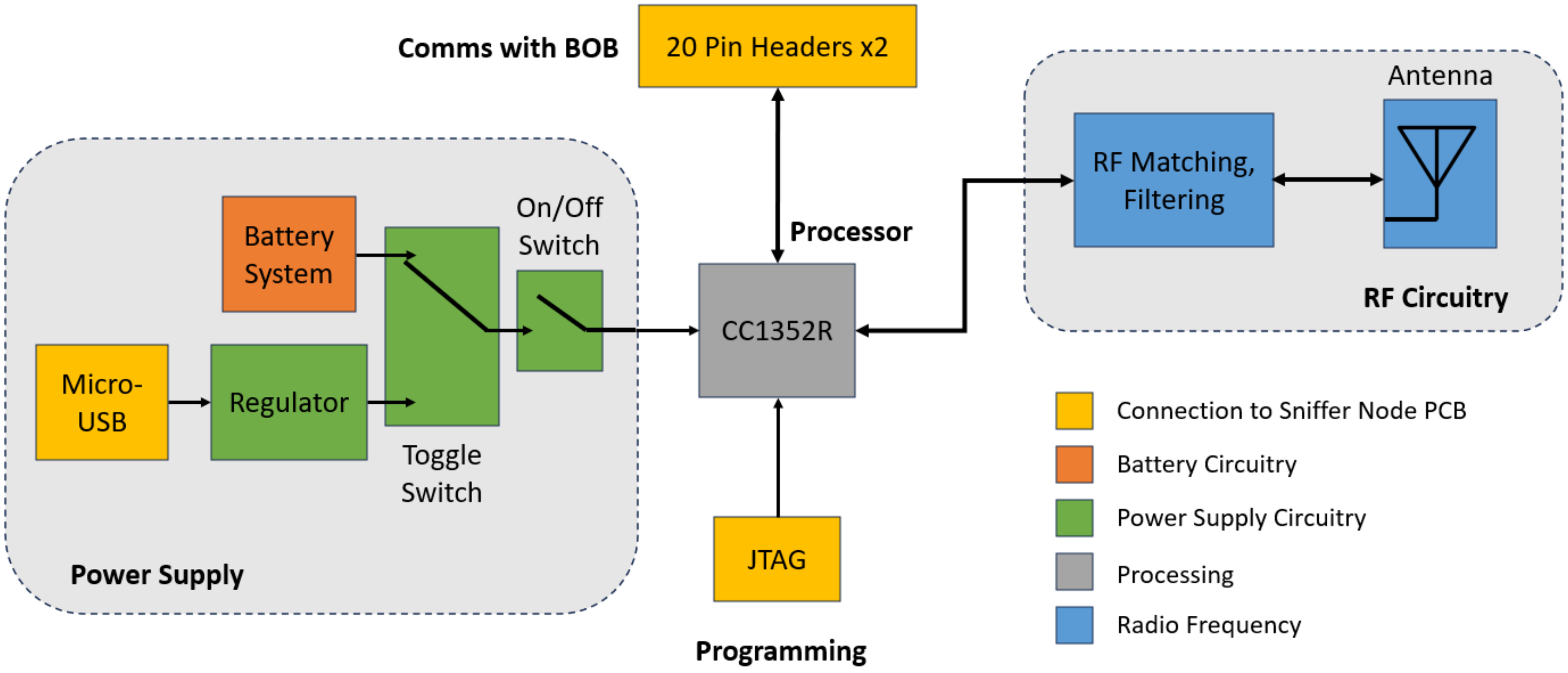
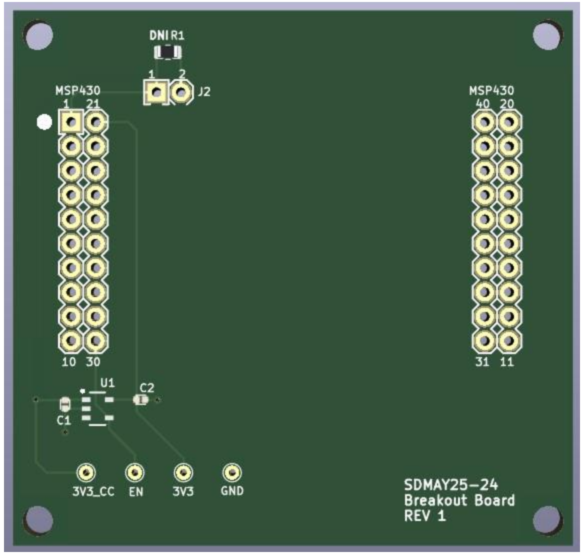
Conceptual Design Diagram - Hardware



Prototype Implementations - Hardware

Breakout Board was designed to eliminate unknowns with the MSP_Simplified

- Load Switch
- Connector spacing
- First order with KiCAD
- Grad Student testing



Breakout Board Revision 1

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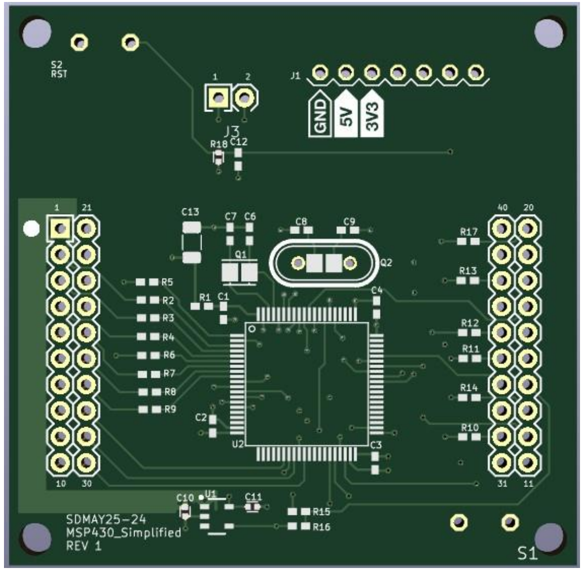
Prototype Implementations - Hardware

- Removed Debugger Logic
- DNP for unused GPIOS
- Load Switch for CC1352 rail
- PCB Dimensions



MSP_Simplified Revision 1

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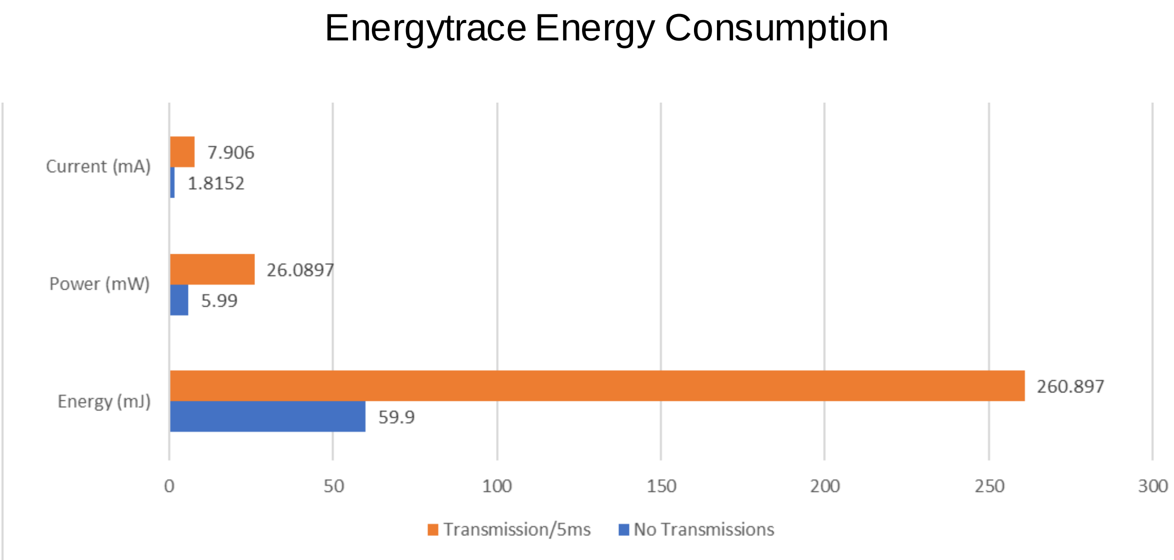
Prototype Implementations - Hardware



Max sample time: 10s
Voltage: 3.3V

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Prototype Implementations - Hardware

Rechargeable LIPO Battery

- 2.8 V - 3.6 V typical output

- Using voltages, required capacity ~ 820 - 1060 mAh
- Range of capacities available with many in needed range

- Charger on board sniffer

Pros:

- High capacity
- Sustainable
- No replacement of batt.
- High voltage supplied

Cons:

- Electronics complexity
- Mechanical complexity
- Design time

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Prototype Implementations - Software Timing

Parameter Given:

One 8-byte packet every 5ms

Array Based Queue:

Holds up to 2500 10 bytes packets

Test Observations:

12ms to send a max packet length 128 bytes

Band Swapping:

~30ms to swap bands

Time(ms)	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95	100
Odd									From BOB to Sink Band											
Odd(Bytes)	8	16	24	32	40	48	56	64	64	64	64	64	64	64			0	0	0	0
Even		From Sink to BOB Band																		
Even(Bytes)	0	0	0	0	0	0	0	8	16	24	32	40	48	56	64	72	80	88	96	104

Time(ms)	105	110	115	120	125	130	135	140	145	150	155	160	165	170	175	180	185	190	195	200
Odd		From Sink to BOB Band																		
Odd(Bytes)	0							8	16	24	32	40	48	56	64	72	80	88	96	104
Even									From BOB to Sink Band											
Even(Bytes)	112	120	128	136	144	152	160	168	168	168	168	168	168	168			40			0

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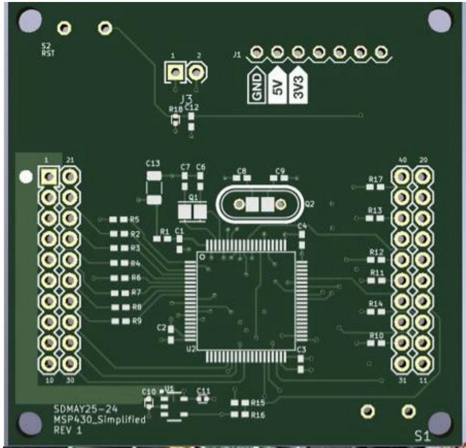
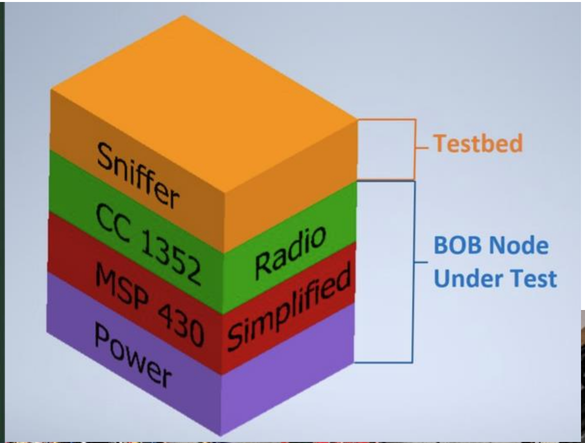
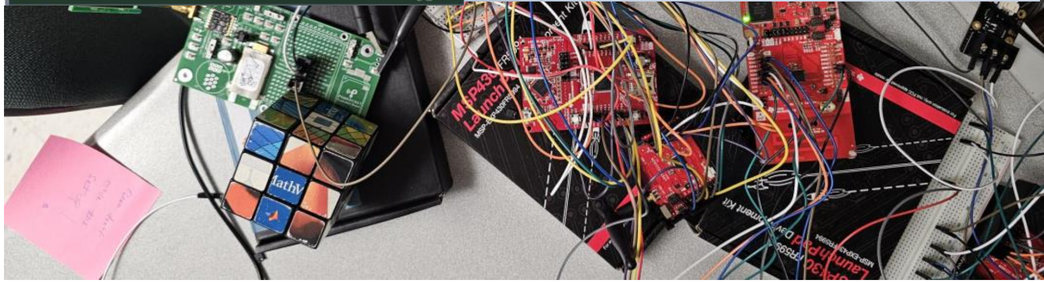
Design Complexity

Design Elements Discussed:
- PCB design
- PCB stacked integration
- Software Timing
- EnergyTrace Battery Consumption

Design Iterations:
- PCB Breakout Board
- Tester battery system
- Sniffer Communications







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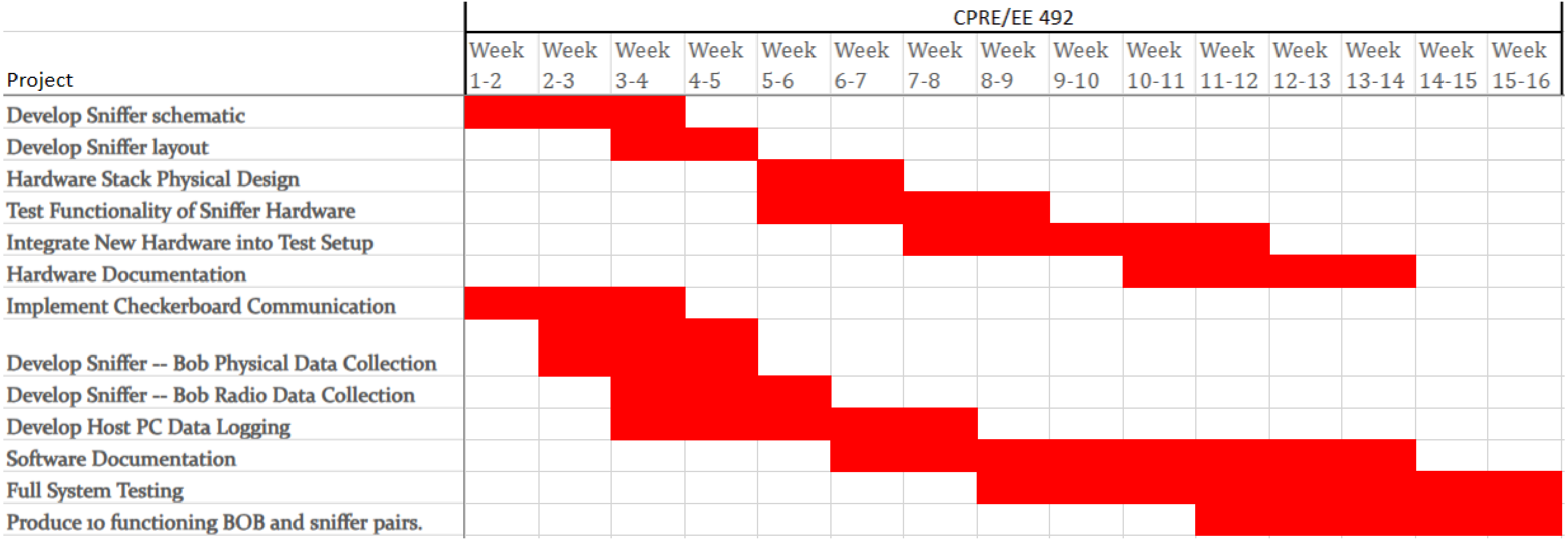
Project Plan – Schedule/Milestones



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Risk Mitigation

- Band-switching non-functional -> Swap to two CC1352 implementation
- Custom hardware non-functional -> Return to using off-the-shelf boards
- Hardware orders delayed -> Order ASAP
- Hardware becomes damaged -> Have extras on-hand

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Test Plan – Unit Testing

Hardware
- Visual inspection, benchtop tools, units of test code
- Test plans generated for each board
- Isolation, power supply, programmability, communication, specific functionality

Software
- Test activation of all interrupts
- Time-based interrupts
- Receive based interrupts
- Queue loading and emptying

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Test Plan – Interface/Integration

Hardware

- Inputs and outputs (antenna, headers) with test code and probing as needed
- Test isolation and power supply with all PCBs connected

Software

- UART
- Radio
- GPIO
- Interrupt Integration

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Test Plan – System Level

Elements to test: Functionality, Accuracy, Usability

Mock BOB Emulation

1. Ensure system functions and network communicates - **Functionality**
2. Compare against old system with identical tests – **Accuracy**

Implementation Testing

1. Test system with research team's setup – **Functional**
2. Hand off system with documentation to researchers - **Usability**

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Thank you!

Hardware Cost Estimates

Cost for Single Board										
Item #	Designator	Manufacturer	Mfg Part #	Description / Value	Package	Supplier	Link	Qty	Cost	Total Cost
1	U1	GLF Integrated Power	GLF1111	Power Switch/Driver P-Channel 2A	SOT-23-5L	DigiKey	https://www.di	1	0.33	0.33
2	C1, C2	Samsung Electro-Mechanics	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	0402	DigiKey	https://www.di	2	0.01	0.02
3	J1	Samtec Inc.	SSW-110-03-G-D	CONN RCPT 20POS 0.1 GOLD PCB	-	DigiKey	https://www.di	2	3.89	7.78
4	J2	Molex	22122024	TH, Right Angle 2 position 0.100" (2.54mm)	-	DigiKey	https://www.di	1	0.77	0.77
5	R1	Stackpole Electronics	RMCF0805ZT0R00	RES 0 OHM JUMPER 1/8W 0805	0805	DigiKey	https://www.di	1	0.018	0.018
6	-	-	-	Board Fabrication	-	JLCPCB	-	1	3.892	3.892
								Total Cost		12.48

Cost Per Breakout Board

Cost for single board										
Item #	Designator	Manufacturer	Mfg Part #	Description / Value	Package	Supplier	Link	Qty	Cost	Total Cost
1	U1	GLF Integrated Power	GLF1111	Power Switch/Driver P-Channel 2A	SOT-23-5L	DigiKey	https://www	1	0.33	0.33
2	C1, C2, C3, C4, C10, C11	TDK Corporation	C1005X5R1A104M050BA	CAP CER 0.1UF 10V X5R 0402	0402	DigiKey	C1005X5R1A	6	0.021	0.126
3	J2	Samtec Inc.	SSW-110-03-G-D	CONN RCPT 20POS 0.1 GOLD PCB		DigiKey	SSW-110-03	2	3.89	7.78
4	J3	Molex	22122024	TH, Right Angle 2 position 0.100" (2.54mm)	-	DigiKey	https://www	1	0.64	0.64
5	C6, C7	TDK Corporation	C1005C0G1H220J050BA	CAP CER 22PF 50V C0G 0402	0402	DigiKey	C1005C0G1H	2	0.047	0.094
6	C12	TDK Corporation	C1005X7R1H102K050BA	CAP CER 1000PF 50V X7R 0402	0402	DigiKey	C1005X7R1H	1	0.051	0.051
7	C13	Murata Electronics	GRM155R61A106ME11D	CAP CER 10UF 10V X5R 0402	0402	DigiKey	GRM155R61A	1	0.091	0.091
8	J1	Sullins Connector Solutio	PRPC007SBAN-M71RC	CONN HEADER R/A 7POS 2.54MM	-	DigiKey	PRPC007SBA	1	0.191	0.191
9	Q1	EPSON	FC-135R 32.7680KA-A0	CRYSTAL 32.7680KHZ 12.5PF SMD	-	DigiKey	FC-135R 32	1	0.7	0.7
10	R1, R2, R3, R4, R5, R6, R	YAGEO	RC0402JR-070RL	RES 0 OHM JUMPER 1/16W 0402	0402	DigiKey	RC0402JR-0	17	0.0045	0.0765
11	R18	YAGEO	RC0402FR-0747KL	RES 47K OHM 1% 1/16W 0402	0402	DigiKey	RC0402FR-0	1	0.015	0.015
12	U2	Texas Instruments	MSP430FR5994IPN	IC MCU 16BIT 256KB FRAM 80LQFP	-	Mouser	MSP430FR59	1	11.27	11.27
13	Q2	DNP								
14	-	Würth Elektronik	60900213421	JUMPER W/TEST PNT 1X2PINS 2.54MM	-	DigiKey	6090021342	1	0.31	0.31
15	S1,S2	E-Switch	TL59NF160Q	SWITCH TACTILE SPST-NO 0.05A 12V	-	DigiKey	TL59NF160Q	2	0.284	0.568
16	J2 (trying another comp	Samtec Inc.	SSW-110-23-G-D	CONN RCPT 20POS 0.1 GOLD PCB	-	DigiKey	SSW-110-23	0	5.71	0
17	-	-	-	PCB Fabrication	-	JLCPCB	-	1	4.96	4.96
								Total Cost		27.2025

Cost Per MSP Simplified Single Board Cost

Approximate Cost Per Board	
Breakout Board	~$13
MSP Simplified	~$28

Literature Study

- "Experimental Study of Lifecycle Management Protocols for Batteryless Intermittent Communication"[2]

- "Toward a Shared Sense of Time for a Network of Batteryless, Intermittently-powered Nodes"[3]

- "Reliable Timekeeping for Intermittent Computing"[4]

Stack Pinouts

SD)

Table 1

GPIO	MSP430	CC1352 radio	I/O (as seen from the msp)
Data Received	P5.0	DIO22	I
Transmit Request	P5.1	DIO3	O
Transmit Done	P5.2	DIO24	I
SPI Master Ready	P5.3	DIO19	O
SPI Slave Ready	P5.4	DIO7	I
FRAM Written	P5.5	DIO11	O
Power radio	PJ.4		
SPI MOSI	P6.4	DIO9	
SPI MISO	P6.5	DIO8	
SPI CLK	P6.6	DIO10	
SPI SS	P6.7	DIO20	O

Table 2

GPIO	MSP430	CC1352 radio	CC1352 sniffer		Harvester	I/O
Powered ON	P7.7		DIO25	DIO28		O
Event Gen	P7.4		DIO26	DIO29		I
Testbed Reset	P7.5		DIO27	DIO30		I
Easylink Tx		DIO25	DIO24	DIO21		
Event drop	P7.6		DIO9	DIO8		O
Reset	P7.3				Reset	I

Note currently in our setup we have only one sniffer for two msp430 nodes. I/O are defined with respect to msp430 node

Code needs update

Figure 12: Plan to Create Extra NC Pins on the CC1352R Development Board

Stack Pinouts

MSP Board Pinout							
Pin #	Func	Pin #	Func	Pin #	Func	Pin #	Func
1	3V3 to CC	21	3V3	40	P5.4	20	GND
2	GPIO	22	GND	39	GPIO	19	P5.1
3	GPIO	23	NC	38	P6.7	18	P5.5
4	GPIO	24	GPIO	37	P3.5	17	GPIO/EN
5	P5.0	25	GPIO	36	GPIO	16	NC
6	P5.2	26	GPIO	35	GPIO	15	P6.4
7	P6.6 (SPI)	27	GPIO	34	RST_MSP	14	P6.5
8	P1.0	28	P7.3	33	P1.1	13	P1.6
9	P7.4	29	P7.5	32	P1.7	12	P2.6
10	P7.6	30	P7.7	31	P2.5	11	GPIO

Figure 14: MSP Simplified Pinout

Stack Pinouts

Harvester Board Pinout							
Pin #	Func	Pin #	Func	Pin #	Func	Pin #	Func
1	NC	21	3V3	40	P5.4	20	GND
2		22	GND	39		19	P5.1
3		23	NC	38	P6.7	18	P5.5
4		24		37	P3.5	17	
5	P5.0	25		36		16	NC
6	P5.2	26		35		15	P6.4
7	P6.6	27		34		14	P6.5
8	P1.0	28	P7.3	33	P1.1	13	P1.6
9	P7.4	29	P7.5	32	P1.7	12	P2.6
10	P7.6	30	P7.7	31	P2.5	11	

Figure 15: Power Harvester Pinout

LIPO Cost Estimate (Slightly Outdated)

Item	Cost per Item	Quantity	Total Cost
LIPO	$5.00	10	$50.00
Battery Mount	$3.00	10	$30.00
Protection/Management ICs	$0.50	10	$5.00
Charger ICs and parts	$1.00	10	$10.00
Charger PCB	$15.00	1	$15.00

Cost per board: $11.00

Updated cost per board (no charging board): $9.5

Time Skew Analysis

CC1352 clock was ran with constant time reporting, compared to real-time clock

Skew ended up > .005%, .01% between any given 2 nodes

Two nodes skewing in opposite directions: take 50 seconds to skew by 5 ms

Prototype Implementations - ????

No Transmit	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

Transmit every 5ms	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

$$P_{avg} = 0.5(5.99) + 0.5(26.09) = 16.04mW$$

$$E_{wk} = P_{avg}(7)(24)(60)(60) = 9.701kJ$$

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Prototype Implementations - ????

No Transmit	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

Transmit every 5ms	Min	Max	Mean
Power (mW)	4.6707	7.5945	5.9900
Current (mA)	1.4154	2.3014	1.8152

$$capacity-needed = (0.5(I_{normal}) + 0.5(I_{trans,5ms}))(7)(24)$$

$$capacity-needed = ((0.5)(1.8152) + (0.5)(7.9060))(7)(24) = 816.581\,mAh$$

$$capacity-needed = (\frac{P_{avg}}{V_{supplied}})(7)(24) = \frac{2695}{V_{supplied}}\,mAh$$

+10% buffer

p. 37-38

References

[1] “CC13xx/CC26xx Hardware Configuration and PCB Design Considerations.” Accessed: Dec. 04, 2023. [Online]. Available: https://www.ti.com/lit/an/swra640g/swra640g.pdf?ts=1701669788758&ref_url=https%253A%252F%252Fwww.google.com%252F

[2] V. Deep et al., "Experimental Study of Lifecycle Management Protocols for Batteryless Intermittent Communication," 2021 IEEE 18th International Conference on Mobile Ad Hoc and Smart Systems (MASS), Denver, CO, USA, 2021, pp. 355-363, doi: 10.1109/MASS52906.2021.00052.

[3] V. Deep, M. L. Wymore, D. Qiao and H. Duwe, "Toward a Shared Sense of Time for a Network of Batteryless, Intermittently-powered Nodes," 2022 IEEE International Performance, Computing, and Communications Conference (IPCCC), Austin, TX, USA, 2022, pp. 138-146, doi: 10.1109/IPCCC55026.2022.9894317.

[4] Jasper de Winkel, Carlo Delle Donne, Kasim Sinan Yildirim, Przemysław Pawełczak, and Josiah Hester. 2020. Reliable Timekeeping for Intermittent Computing. In Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '20). Association for Computing Machinery, New York, NY, USA, 53–67. https://doi.org/10.1145/3373376.3378464